IN THE CLAIMS

1. (Original) A method of providing a switching point voltage for an integrated circuit by using a differential input buffer circuit, comprising:

determining available first and second reference voltages in the integrated circuit;

computing a switching point voltage based on the available first and second reference voltages to maximize high and low noise margins of the integrated circuit; and

setting the switching point voltage by sizing transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to a supply voltage node and the first and second reference voltages based on the computed switching point voltage.

2. (Original) The method of claim 1, further comprising:

sizing transistors in the differential input buffer to a specific speed of operation based on a load driven by the differential input buffer.

3. (Original) The method of claim 1, wherein computing the switching point voltage comprises computing the switching point voltage based on ((first reference voltage + second reference voltage)/2).

4. (Original) A method of providing a switching point voltage for an integrated circuit by using a differential input buffer circuit, comprising:

determining available first and second reference voltages in the integrated circuit using a supply voltage as the first reference voltage;

computing a switching point voltage based on the available first and second reference voltages to maximize high and low noise margins of the integrated circuit;

setting the switching point voltage by applying the supply voltage across the gate to source voltages of transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to the supply voltage node and the first and second reference voltages based on the computed switching point voltage; and

providing the switching point voltage based on the set switching point voltage.

5. (Original) The method of claim 4, wherein coupling the input stage to the second reference voltage comprises coupling the input stage to ground.

6. (Original) The method of claim 4, wherein computing the switching point voltage comprises computing the switching point voltage based on ((first reference voltage + second reference voltage)/2).

7. (Original) A method of designing a differential input buffer circuit to provide a switching point voltage for an integrated circuit, comprising:

determining a required switching point voltage for the integrated circuit to maximize high and low noise margins of the integrated circuit;

defining required first and second reference voltages based on the determined switching point voltage; and

sizing transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to a supply voltage node and the first and second reference voltages to provide the switching point voltage based on the defined first and second reference voltages to maximize high and low noise margins.

8. (Original) The method of claim 7, wherein determining a required switching point voltage for the integrated circuit comprises averaging the first and second reference voltages.

9-24 (Canceled)

CONCLUSION

Claims 9-24 have been canceled. Claims 1-8 are therefor now pending. The Examiner is invited to contact, Kash Nama at (603) 888-7958 with any questions regarding the present application.

Respectfully Submitted,

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